Journal of Nonlinear Analysis and Optimization
Vol. 13(3) (2022), March 2022
https://ph03.tci-thaijjo.org/
ISSN : 1906-9685

J.Nonlinear Anal. Optim

Modified Partial Product Bypassing Multiplier for High Speed DSP Applications

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***Abstract*- A modified approach of generating partial product for successful multiplication of the bit streams has been introduced here paper. The proposed method effectively reduces the multiplication time cycles from NxN to 2N cycles, where N is the bit width of the input. A Carry Save Adder (CSA) tree with a register memory is used to generate the modified Partial product sequence. The shifter mechanism of the multiplier is altered in a way, which the number of total computation cycles can be reduced from 2N to number of 1's present in the multiplicand. The partial product generation mechanism is skipped with the low level input sequence, which further reduces the time complexity. The performance comparison of the proposed bit serial multiplier will be evaluated with the previous literature multiplier using Quartus II Synthesizer.**

***Keywords*- CSA, Bit Serial Multiplier, Quartus II Synthesizer, Partial Product.**

I. Introduction

Utilizing the efficient hardware structure in a VLSI chip has main impact on overall cost [1-4]. Given that the hardware can only perform a relatively simple and primitive set of Boolean operations, arithmetic operations are based on a hierarchy of operations that are built upon the simple ones. Since speed, power and chip area are the most often used measures of the efficiency of an algorithm. Algorithm alone has the dominant impact on hardware structure, a scalable architecture requires reprogrammable multiplexer which increases hardware size. The battery-operated multimedia devices require energy-efficient circuits, particularly digital multipliers which are building blocks of Digital Signal Processors (DSP). Adders and subtractors are basic arithmetic unit to achieve multiplier and divisor in DSP applications, e.g., FFT/IFFT, Digital Cosine Transform (DCT), digital filtering, etc [1]. Hence, it is proposed to detect the bitwise nullity of the multiplicand in the vertical direction. The partial product in the horizontal direction in an array multiplier to remove the unnecessary operations taking place in the corresponding adding cells. The hardware implementation of a multiplication operation consists of three stages, the generation of Partial Products (PPs), the reduction of PPs and the final carry- propagation addition [2]. The partial products can be generated either in parallel or serially, depending on the target application and the availability of input data. The partial products are generally reduced by Carry-Save Adders (CSAs) using an array or a tree structure. Carry propagation addition is compulsory when the number of partial products is reduced to two rows. This final adder can be a simple Ripple Carry Adder (RCA) for low power or a Carry Look-Ahead Adder (CLA) for high speed [2]. As the height of PP tree increases linearly with the word length of the multiplier, it achieves the area, delay and power dissipation of the two subsequent stages.

II. Existing Method

The structure manages to reduce the power dissipation by an observation that the energy consumption of CMOS logic is proportional to the number of transitions. J.Ohbanetal proposed a "bypassing" multiplier which skips the addition when the partial product of a row is zero. H.C.Chowetal proposed a signed 2-dimensional bypassing approach detecting the nullity of the partial products as well as the multiplicand at the same time to determine whether the additions on the corresponding rowand those on the corresponding column are skipped or not, respectively.

A. Baugh-Wooley algorithm:

A Baugh Wooley algorithm is much optimized to handle the sign bits and this Baugh Wooley multiplier is designed by ordinary multiplier for 2's complement numbers and it is a hierarchical approach. This multiplier needs two inputs, and this

type is signed representing the multipliers and multiplicand and one output P of type signed representing the product. A typical signed multiplication is based upon the following equations.

III. PROPOSED METHOD

A. High Speed Low Power Multiplier:

A bypassing power aware signed multiplier is frequently utilized in FFT/IFFT operation. A Baugh wooley algorithm using bypassing cells is designed to skip the entire byte operation when the horizontal or vertical partial product is zero. This total number of operating cycles required is 2N where N is the order of multiplier. A modified design of altering Partial Product generation method to achieve the entire multiplicative operation in N cycles rather than 2N cycles is proposed. An asynchronous on the fly multiplier method is used to modify the Partial Product(PP) generation in more convenient way. The existing methodology of on the fly accumulation multiplier for lesser operating cycles is modified in a way like integrating the bypassing methodology of Baugh Wooley multiplier. By scanning the possibilities of zero occurrences in both of operand and also during the partial product generation the entire operation is skipped to handle the next high operating bit which results in increased speed and reduced power.

B. Modified Partial Product Generation:

A new technique of generating the individual row of partial products by considering two serial inputs, one starting from the LSB and the other from MSB. Using this feeding sequence and the proposed counter-based accumulation technique presented in Section III, it takes only cycles to complete the entire partial product generation and accumulation process for nxn multiplication. The theoretical underpinning of this design is elaborated as follows. The product of two -bit unsigned binary numbers and can be expressed as

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