



Design and Implementation of High Voltage Tolerant I/O Buffers with Low-Voltage CMOS Process for PCI Application in 180nm technology

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Advances in silicon fabrication technology have assisted in satisfying the computing industry's demands for increased speed, reduced power consumption and have also presented new and complex challenges to circuit designers. In CMOS technology, reduction in gate oxide thickness improves speed of operation, but imposes a limit on allowable electric field stress on the gate oxide. This limit is very critical to IO circuits containing MOS elements that experience spurious noise, overshoots and undershoots due to transmission line effects. The problem of gate oxide is worse when the transmission line carries high voltage and that high voltage interfaces with a Low voltage signal then the circuits having MOS element may suffer from Gate Oxide Stress, Leakage currents, overshoot, under shoot and signal reflection.

An I/O Buffer architecture is demonstrated which provides fast output transitions and efficient voltage level shifting. The buffer contains a gate tracking circuit which damps ringing associated with supply bounce and can be used in the mixed signal environment 1.8V/2.5V. The proposed buffer has inverter and PMOS connected parallel to the load to drive large currents. The proposed buffer eliminates gate-oxide overstress, leakage currents, overshoot, undershoot, signal reflection, output to supply current flow when common bus voltage is higher than the supply voltage and has no leakage paths in the I/O circuit. While this paper discusses about 1.8V/2.5V supply combinations as an example, the same circuit topology can be used for other mixed supply combination like 2.5V/5V, 3.3V/5.5V.

The modified (I/O) cell drastically reduces the I/O power by 13.71%. The maximum operating clock is 150 MHz to drive a 20-pF offchip load. Physical measurements of the proposed I/O cells show that the delay of the proposed buffer is 1.3ns. Over and above the power saving feature, the proposed buffer occupies merely 307.2 μ m², lower than any prior commercially available I/O buffers.

1. Introduction

In mixed voltage interfaces, several devices fabricated in various technologies, communicate using the common signal bus. The conventional CMOS output buffers are not suitable for such applications as they suffer from gate-oxide overstress [1] and leakage current [2]-[3] that can cause hazardous latch up problems.

Figure 1 explains how gate oxide stress occurs in I/O buffers. Conventional CMOS output buffer is shown in figure 1. Supply voltage V_{dd} is 3.3V. P0 and N0 are PMOS pull up and NMOS pull down transistors respectively. When enable signal (OE) is 3.3V, output buffer operates in transmit mode and output signal (PAD) varies according to input signal (Din). When OE signal is 0V (in tri-state mode), the pre-driver turns off P0 and N0 by driving the gate voltages to 3.3V and 0V respectively. In this mode, the PAD signal can rise to 5.5V because other peripheral device having 5.5V supply is driving the common bus. When PAD rises to 5.5V, N0 suffers from overstress voltage ($|V_{gd}| = 5.5V$, $|V_{ds}| = 5.5V$). The gate oxide may become leaky due to tunneling effect and/or dielectric breakdown. It may even be damaged permanently due to large electric field across the gate oxide.

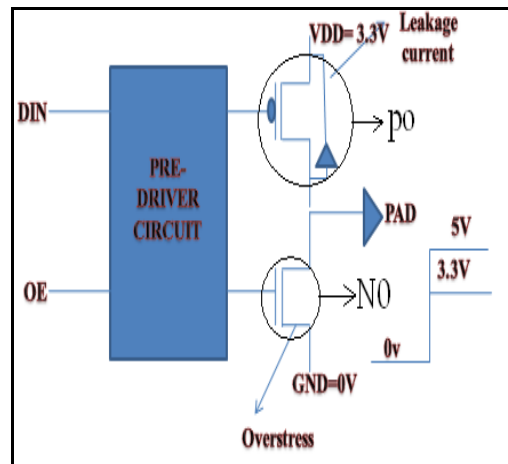


Figure 1 Gate oxide stress in I/O

Recently, several techniques have been proposed to reduce overshoot, undershoot and gate oxide over stress many techniques have been proposed. NMOS configuration [4]-[11] is used. Again due to 5.5V at common bus Figure 1, the parasitic drain-well junction diode of P0 from figure 1 becomes forward biased and P0 itself also starts conducting. Both cause leakage current path from PAD to Vdd. To prevent the leakage current from PAD to Vdd, output buffer with gate tracking circuit and floating N-well [8]-[14] has been reported. But it is preferred to connect N-well always to a defined potential.

In circuit [3] during tri-state mode, when PAD voltage becomes higher than Vdd, both N-well and gate 23 are connected to PAD and when the PAD voltage becomes lower than Vdd, both of them are connected to Vdd. However, in transmit mode, N-well is always connected to Vdd. The paper [3] has special circuitry called Bulk control circuitry which forms an closed circuit to connect the gate to the pad when the pad voltage is outside the range of supply voltages so that non conducting path is created through the pair of second polarity-type transistors. This allows the pad to remain in high impedance state even when the pad voltage is outside the range of supply voltage. This technique reduces gate overstress which may reduce ESD. But only disadvantage is current driving capability is too low and slow rise time. To overcome this disadvantage a proposed buffer is made where a inverter and PMOS are given parallel to the output driver. So that it can drive large amount of current and can have faster rise time.

2. DESIGN PRINCIPLE OF I/O BUFFERS

The dynamic N-well bias circuit used to control the Nwell voltage i.e. transistors is shown in figure 2. When output buffer operates in transmit mode (OE is 3.3V), N-well is always connected to Vdd. In tri-state mode (OE is 0V), when PAD is driven higher than Vdd, to turn off the parasitic drain-well junction diode, N-well is connected to PAD. However, when PAD becomes lower than Vdd in tri-state mode, N-well is connected to Vdd.

2.1 Transmit Mode

When enabled (oe), the I/O circuit basically consists of series-connected NMOS transistors 21 and 22 (Fig .2), which function as the pull-down devices and series-connected PMOS pull up transistor 23 is driven by the output of the NAND logic gate 62, which inverts the signal at the din. The gate of NMOS pull down transistor 22 is always tied to the supply (+1.8V) and the gate of the other NMOS pull down transistor 21 is driven by the NOR logic gate, which also inverts the signal at the input node din. Note that the PMOS transistor 53 is turned on with the node 30 low to ensure that the common bulk, the N-well regions, connection to the PMOS transistors 23-24 and 51-53 is tied to the VDD supply (+1.8V) for operation of these transistors. The PMOS transistors 51 and 52 are turned off during this mode of operation. The width and length of PMOS and NMOS transistor for the given specification is calculated by using the width to length ratios are calculated using NMOS and PMOS linear current equations based on specifications shown in table 1

Table 1 Specification for high voltage tolerant I/O buffer

Sl. No.	Specification	Actual
1.	VDD	1.8V
2.	VSS	0V
3.	VPAD Max	5V

4.	VPAD MIN	-5V
5.	C _{load}	10pF
6.	Voltage translation	1.8-2.5 V/2.5-3.3V/3.3-5V
7.	Working frequency	125MHz
8.	Power dissipation	7.985*10-8 Watts
9.	Area	291 um2

VTP=0.3V, VTN =0.3V, NMOS Linear current equation is

$$I_{ds} = \frac{\mu_n C_{ox} W_n}{2L_n} \{2(V_{gs} - V_T)V_{ds} - V_{ds}^2\} \dots (Eq.1) \text{ PMOS Linear current equation}$$

$$I_{ds} = \frac{\mu_p C_{ox} W_p}{2L_p} \{2(V_{gs} - V_T)V_{ds} - V_{ds}^2\} \dots (Eq.2) \text{ Solving these equations}$$

$$\frac{W_n}{L_n} = \frac{\mu_p}{\mu_n} \left[\frac{(V_{dd} + V_{tp} - V_{sat})}{\{V_{sat} - V_{tn}\}} \right]^2 \dots (Eq.3)$$

Where,

$$\mu_n = 2.5\mu_p, L_p = L_n \text{ and } V_{DD} = 1.8.$$

$$V_{SAT} = \frac{\mu_p (V_{IL} + V_{IH})}{\mu_n} = 1.345$$

Solving these equation's Eq.1, Eq.2 and Eq.3 for PMOS and NMOS for the specifications in Table 2 the required Width to Length ratios for the transistors in the I/O buffer can be computed.

Table 2 Width to length ratios of I/O buffer

Logic circuit	Wp/Wn (μ)
Output stage	16u/8u
Pre-Driver (Nand- Nor)	4u/1u – 8u/4u
Inverter and PMOS	4u/2u and 6u
Switch Circuit	2u

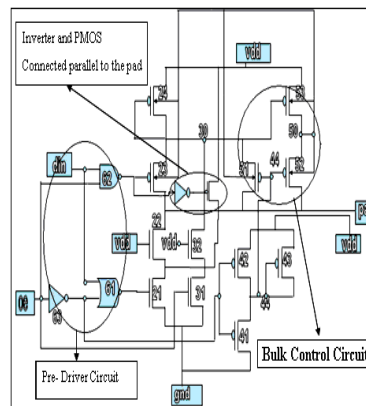


Figure 2 Proposed CMOS I/O Buffer

2.2 Tri-state Mode:

When the I/O circuit is disabled, there are two basic concerns

- The node 20 and pad 13 remain in a high-impedance state over the entire range of voltages, 0 to 2.5V, applied to the pad, i.e., there are no leakage paths in the I/O circuit.
- The second concern is that no element in the I/O circuit is damaged due to high voltages across the gate oxide of any MOS transistor of the I/O circuit.

With respect to high impedance aspect of the I/O circuit, it should be noted that the node 44 goes to (vdd-vth) in the disable mode. The logic signals to the gate of the PMOS PULLUP transistor 23 is high and the logic signals to the gate of the NMOS PULLDOWN transistor 21 is low. Both transistors are normally off. Nonetheless, a concern is that the gate (VDD) for the PMOS transistor 23 may not be sufficient to turn off the transistor 23 when the voltage on the pad 13 exceeds VDD+vth. This is alleviated by the series-connected PMOS transistor 24. Regardless of the state of the PMOS transistor 23, the second PMOS pullup transistor is always off and non-conducting. This ensures that there is no current flow from the pad 13 to the voltage supplies. To ensure that the PMOS transistor 23-24 and 51-53 operate as stated above, voltages of the N-type bulk of these transistors should be controlled such that

The transistor operates correctly. When the voltage on the pad goes to 2.5V, forward-biased PN junctions connected to the pad 13 are avoided. Such PN junction reduce the impedance of the pad13, as well as possible activating parasitic bipolar structures which may lead to higher current flow, or latchup. Either possibility is undesirable.

Case a: PAD > (Vdd + |Vtp|): When pad greater than VDD, the PMOS transistor 52 turns on to connect the node 50 to the pad. This ensures that all transistors operate as described above. Fig. 4.5 helps illustrates the operation of the I/O circuit by the plots of the voltages at various nodes, specifically , the control node 18, the pad (node 20), node 50, and Vsub-vg for PMOS transistor 23.

With respect to avoidance of high voltages across the gate oxides of any of the MOS transistors in the I/O circuit to prevent damage, it should be noted that the described I/O circuit has no transistors with gates which are connected directly to the pad. The NMOS transistor 22 and 32, which are cascade-connected, both limit the voltage at their sources, as well as their gate-to-drain voltages. All other transistors which are connected to the pad 14 (i.e., pad, the PMOS transistor 23, 51, 52) have gates which are tied to the supply voltage VDD during the high-impedance state when high pad voltages occur. The PMOS transistor 53 and 24 has gate voltages which track the voltage on the pad when the voltages on the pad go very high in excess of 2.5V. Hence voltage across the transistor gate oxides are minimized.

Case b: PAD < (Vdd + |Vtp|): when pad is lower than VDD, 1.8V, the PMOS transistors 51 and 52 are switched off. This allows the node 50 which is connected to the N-type bulk regions of the PMOS transistors 23-24 and 51-53 to float with in well constrained voltage limits. The node 50 cannot float too low since this is limited by the action of the PN junctions in which the p-doped region is tied to VDD will then turn on and keep the node 50 at VDD. The below wave form is shown during the transmit mode. Figure 3 shows the simulation result in transmit and tri-state mode.

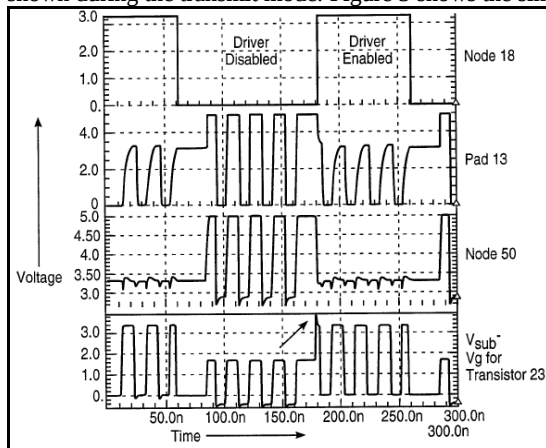


Figure 3 Simulation in transmit and tri-state mode

Figure 3 helps in illustrating the operation of the I/O circuit by the plots of the voltages at various nodes, specifically, the control node 18, the pad 13 (node 20), node 50, and, and Vsub-vg for PMOS transistor 23(the difference between the voltages at node 50 and the gate).

Here worst case scenario occurs when the voltage on the pad 13 has been driven high and the node 50 connected to the N-type bulk regions is also high (+2.5V) as well, while the I/O circuit has been disabled. The I/O circuit is enabled, the output from the NAND logic gate 62 may be immediately driven low (0V). the node 50 drops toward VDD (1.8V) but may do slowly. This may momentarily cause a large potential difference between the gate and bulk/drain of the PMOS

pullup transistor 23. However, as shown by an arrow 70 in figure 3, this voltage is held to less than 2 Volts with proper sizing of the transistors to avoid jeopardizing the integrity of the gate oxide of PMOS transistor 23.

3. TEMPERATURE ANALYSIS

This analysis has been carried for commercial range of -25 degrees to 125 degrees. This has been carried out because normally all devices work properly in room temperatures. But when temperature decreases or increases i.e, more negative temperatures and more positive temperatures then there is a possibility of device not working. So, this analysis has been carried out to ensure that device works properly even at more negative temperatures and also more positive temperatures and the analysis has been carried out between conventional and modified buffers so, it is shown that modified is better than conventional with respect to delay and also the current driving capability which is shown in section. With increase in temperature rise time degrades. But, in proposed buffer which is shown in Table 2 (a) and 2 (b) indicates much faster rise time when compared to the conventional buffer, less delay time and also the faster fall time.

Table 2 (a) Temperature analyses on conventional I/O

temp	td(ns)	power (mw)	tr(ns)	tf(ns)
-25	3.1695	1.6835	2.46	3.7157
0	3.4375	1.5683	2.5849	3.788
25	3.735	1.4668	2.6951	3.877
50	4.0375	1.4266	2.8045	3.9733
75	4.3357	1.4155	2.8952	4.034
100	4.6245	1.3014	2.9987	4.092
125	4.8977	1.202	3.095	4.137

Table 2 (b) Temperature analyses on modified I/O

temp	td(ns)	power (mw)	tr(ns)	tf(ns)
-25	3.01695	2.7835	1.87	2.4157
0	3.3375	2.6683	2.1849	2.688
25	3.635	2.5668	2.1951	2.857
50	4.0045	2.4766	2.3045	2.943
75	4.1357	2.3955	2.352	3.032
100	4.2245	2.3224	2.4187	3.091
125	4.3977	2.2552	2.6	3.107

4. SLEW RATE ANALYSIS

Slew rate analysis is done at varying loads the slew rate is an important indicator of performance of the I/O buffer:

- With increase in slew rate rise time decreases and current increases
- From the above analysis modified buffer is better with respect to rise time and current driving capability. This can be visualized using Figure 5.23 and 5.24 graph. The load current is improved by a factor of more than 30% (**Table 2(a) and 2 (b)**) and the rise time is reduced by a factor of 20% over the conventional buffer (**Table 3(a) and 3(b)**).

Table 3 (a) Slew rate analyses on conventional I/O

I/P			CL 7pf		O/P	I(Ma)
1 W/L=6u	0.1	0.1	2.6	2.5	2.682	4.91
1.8 W/L=6u	0.1	0.1	2.47	2.5	2.682	4.91
2 W/L=6u	0.1	0.1	2.47	2.5	2.681	4.91
2.4 W/L=6u	0.1	0.1	2.47	2.5	2.681	4.97

1						
W/L=6u	0.1	0.1	2.6	2.5	2.682	4.91

Table 3 (b) Slew rate analyses on proposed I/O

I/P			CL 7pf		O/P		I(Ma)
1							
W/L=6u	0.1	0.1	6	2.1	2.5	1.682	7.91
1.8							
W/L=6u	0.1	0.1	6	2.17	2.5	1.682	7.91
2							
W/L=6u	0.1	0.1	6	2.17	2.5	1.681	7.91
2.4							
W/L=6u	0.1	0.1	6	2.17	2.5	1.681	7.97
1							
W/L=6u	0.1	0.1	6	2.1	2.5	1.682	7.91

5. LAYOUT FOR PROPOSED BUFFER

Layout of the designed buffer shows the layout which is shown in **Figure 4** which is manually drawn for the I/O buffer which is integrated as a standard cell. The Pre-driver circuit, output driving circuit, Switch circuit and gate tracking circuit use a “**fingering technique**” to reduce area. For normal layout Bulk contact has to be placed for every 10μ to avoid latch up. The area of the I/O buffer increases due to additional bulk contacts. So, standard cell type design is more area efficient due to single bulk contact for whole circuit. In standard cell bulk contact is made only for VDD and GND. The additional benefit of this approach is that latch up problem is also avoided. The area obtained is in **Figure 4** is 32 μ * 9.6 μ.

When MTCMOS technique was adopted then power has been reduced to $6.89 * 10^{-8}$.

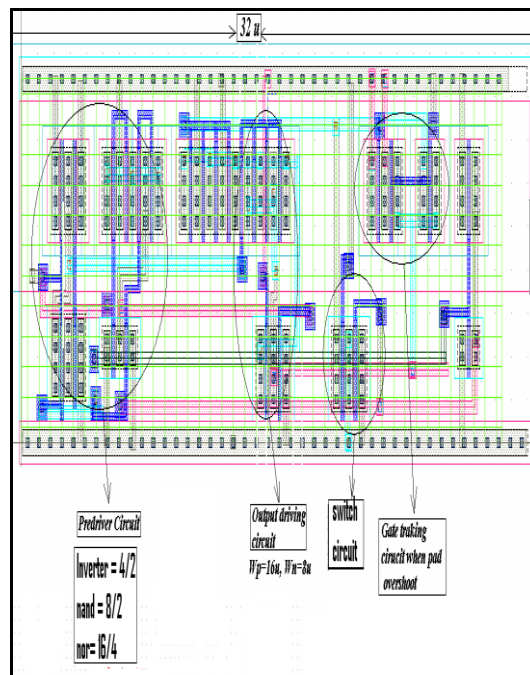


Figure 4 Layout for proposed I/O buffer

6 RESULTS AND DISCUSSION:

Table 4 comparison between Conventional and Proposed Buffer

WN/WP (2)	Conventional Buffer	Proposed Buffer
Offset	+/- 0.3	+/-0.011
Delay (1Pf)	0.9ns	1.2ns
Current (mA)	2.8mA	3.35mA
WN/WP (4)	Conventional Buffer	Proposed Buffer

Offset	+/- 0.35	+/-0.011
Delay(1Pf)	0.7ns	1.1ns
Current (mA)	4.4mA	4.78mA
WN/WP(6)	Conventional Buffer	Proposed Buffer
Offset	+/- 0.35	+/-0.015
Delay(1Pf)	0.6ns	0.7ns
Current (mA)	5mA	7.9mA

Table 5 I/O Derived Specification between Proposed and Actual

I/O SPECIFICATION	Proposed	Actual
VDD	1.8 V	1.8 V
VSS	0V	0V
VPAD Max (V)	5V	5V
VPAD MIN (V)	-5V	-5V
Clod (Pf)	20Pf	10Pf
Voltage translation	1.8-2.5 V/2.5-3.3V/3.3-5V	1.8-2.5 V/2.5-3.3V/3.3-5V
Working frequency (MHz)	150MHz	125MHz
Power dissipation	6.89*10 ⁻⁸	12*10 ⁻⁸
Area (μm ²)	307.2um ²	291um ²
Current driving (Wp/Wn=6u) Max	7.97(mA)	4.97(mA)

Table 4 shows the comparison table where proposed buffer is better than conventional and actual buffer with respect to current driving capability offset and delay even. Table 5 shows the derived versus actual specifications where derived is best only area is more which is basically due to extra inverter and PMOS which is connected parallel to pad.

7. CONCLUSIONS

- Power has been reduced by 13.71% in output buffer using MTCMOS technique.
- Overshoot and undershoot has been reduced by slow discharging of PMOS and NMOS in Nand and Nor circuit respectively.
- Maximum frequency of operation is limited to 150MHz due to inductive effect.
- The buffer can drive a MAX current of 3Ma with a delay of 9ns.
- Bulk control circuit used in I/O buffer leads to reduction in Gate oxide stress.
- The buffer achieves a faster rise time of upto 30% with a 2 times current driving capability due to PMOS and inverter connected in parallel to driving stage
- Output buffer performs level shifting to 1.8V when input voltage changes between (1.8-5)V.

7. REFERENCES

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