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High Speed Parallel Counter Based on State Look Ahead Logic

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Abstract:

Counters are used in circuit operations such as controllers, processors, mobile phone applications, programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Counter architecture design methodologies explore tradeoffs between operating frequency, power consumption, area requirements, and target application specialization. Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, which leads to occurring of delays, more power consumption, so to overcome the drawbacks in existing system I am proposing one parallel counter based on a counting path and state look ahead logic, this phenomena is known as novel pipeline partitioning methodology.

High speed wide range parallel counter that achieves high operating frequencies through using only three simple repeated CMOS-logic module types an initial module generates anticipated counting states for higher significant bit modules through the state look ahead path, D- type flip-flops here d type flip flops are conditional data mapping flip flops simply known as **cdmff** by this low power consumption and high performance can be achieved (the number of transistors are reduced in **cdmff** comparing with simple d flip flop), and 2-bit counters. The state look-ahead path prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously, thus concurrently updating the count state with a uniform delay at all counting path modules/stages with respect to the clock edge. The structure is scalable to arbitrary -bit counter widths (2-to-2N range) using only the three module types and no fan-in or fan-out increase.

We are going to implement this proposed counter using a 0.15- m TSMC digital

cell library and verified maximum operating speeds of 2 and 1.8GHz for 8 and 17-bit counters, respectively. Finally, the area of a sample 8-bit counter was 78125 um2(510 transistors) and consumed 13.89 mW at 2 GHz.

Keywords: State Look Ahead Logic, Parallel Counter, Cdmff