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FPGA Implementation of Digital Beam forming for Phased array RADARs

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Abstract:-

Phased array radar is very important in modern radar development and multiple digital beam forming technology. Beam forming is a signal processing technique used in antenna arrays for directional signal transmission or reception. Digital multiple beam forming on each antenna element about large phased array radar is impossible in processor based digital processing units, because it needs simultaneous processing many A/D channels. In this project we use multi array based beam forming technique with multiplexed signal processing unit on FPGA. The conventional techniques of completely duplicated hardware and also dynamic reconfiguration do not yield the real time parallel beam processing. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. The scope of the work includes the VHDL modelling of 16 element phased array antenna system and RTL implementation of complex NCO, digital mixer, low pass filter, multiplexers, demultiplexers, ROM for coefficient storage and Multiplier unit. The design is functionally verified by simulating the code in ModelSim6.6b from Mentor Graphics. The FPGA synthesis is done using Xilinx ISE (13.2) tool.

KEY WORDS: PowerPc+FPGA, DDC, NCO.

I.INTRODUCTION

Increasing use of antennas in densely populated areas introduces multi-path effects and inter-system interference [4]. Also, low cost technology is expected to result in a proliferation of jamming systems, which is of concern to security and military organizations around the world. The need to reduce such interference is driving improved design of antennas, receivers and processing systems, particularly phased array antennas [2]. Phased array radar advancement has led to unprecedented advances in aerospace platforms and to national defence capability. Phased array radar for airborne platforms is reviewed from a historical and technology viewpoint. The proposed technique in the paper employs multiplexed signal processing unit which is time shared for various beam formers [6]. This technique provides simultaneous beams without any compromise on functionality. The VHDL simulation of all these blocks which were already stated in abstract shall demonstrate the beam formation for multiple beams. Simulated antenna outputs are used to test the developed beam former. The synthesis results of Xilinx ISE (13.2) are analyzed for timing and area. The design and implementation of hardware output i.e. FPGA output shows on Chip scope pro analyzer, Spartan 6E and high speed clock rate as 200MHZ.

II.BACKGROUND

The ability to transmit and receive RF energy in a specific direction plays a crucial role in all radar applications. Forming a beam and electronically scanning it over a range of space can be done using an array of antennas with input/outputs that can be phase shifted with respect to one another. On receiving the signal, phased array beam forming is performed by taking advantage of the time delay of a wave front as it reaches different antenna locations in the array. If the wave front hits the array at an angle, the signal received at an element will be delayed relative to its neighbour by an amount proportional to the element spacing and the angle of incidence. The signal at the m^{th}element will be $s_m(t) = s(t - mt_d)$.

Where $t_d = \frac{x}{c_o} = \frac{\sin(\theta)}{c_o}$ and *co* is the speed of light. To maximize the signal received from a particular direction, a beam forming system imposes a compensating delay, mt_0, on the received signal at the m^{th} element and then combines all M signals to form signal C as described by

$$C = \sum_{m=0}^{M-1} a_m s_m(t + t_0) \qquad (1)$$

Where a_m is an amplitude weighting factor that is sometimes used. When the angle θ is such that $t_d = t_0$, then the delay compensated signals are aligned and they reinforce each other, maximizing C. Wave fronts coming from other angles will have different delays that are not equal to t_0 and the beam former will not align them. Gain can be greatly reduced for those signals.

Generally, the $s_m(t)$ signals are sinusoidal functions with frequency ω and slow (relative to ω) modulations of amplitude and phase. The modulations of amplitude and phase are what carry information about the target. Since $s_m(t)$ is sinusoidal, it is convenient to represent it in terms of a complex signal. It is given as

$$s_m(t) = \mathrm{Re}\{(I + jQ)e^{jw(t - mt_d)}\} \qquad (2)$$

where I and Q are slow functions of time which carry the magnitude and phase information that the receiver is required to detect. When written in the complex signal form, the modified m^{th} signal becomes,

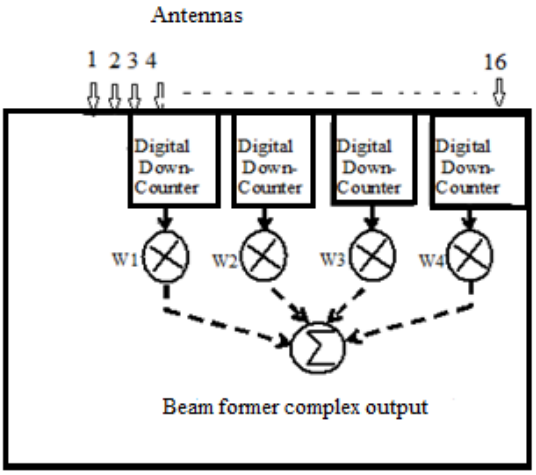
$$a_m s_m(t + t_0) = Re\,(I+jQ)\,(a_m e^{jwmt_o})(e^{jw(t - mt_d)}) \qquad (3)$$

where the second term on the right hand side is a complex weight which includes the amplitude weighting and delay. When the incidence angle θ is such that $t_d = to$, then the m dependent terms in the exponent cancel and all element signals in (1) sum constructively.

In an analog beam former, the weighting and summation operations occur at high frequency whereas a digital beam former performs weighting and summing digitally at baseband frequencies. This paper is focused on digital beam forming, which is gaining in popularity for contemporary radar systems.

III.BLOCK DIAGRAM

We know that a signal is exist in analog form universally. The signals are present at all bands of frequency. So we have to receive a band of signals which are of having our information. To select and to process, we use a device called as Radio Frequency translator simply called as RF Translator. This works in GHZ range and process the signal to low frequency range of 64MHZ. It is performed to remove the spurious channels present at the high frequencies. Then each analog signal is subsequently sampled by an analog-to-digital converter (ADC) which effectively replicates copies of the IF



spectrum at integer multiples of the sampling frequency.

Figure 1: Digital Beam Forming Block Diagram.

The digital signal is down converted to generate Inphase and Quadrature components. It is important to ensure that the pass band reflections do not overlap because this event would lead to a loss of information. After sampling, all processing takes place digitally on the FPGA. The advent of larger and faster Xilinx FPGA's has opened up the field of digital signal processing. The large array of configurable logic blocks within the FPGA give great flexibility together with speed, once configured the FPGA is not as flexible as a processor but is much faster. For many DSP applications speed is important especially for the initial processing of the data, after which the data rate reduces and becomes more manageable. Digital down Conversion is a technique that takes a band limited high sample rate digitised signal, mixes the signal to a lower frequency and reduces the sample rate while retaining all the information.

i. Digital down Converter

Digital down Conversion is a technique that processes a band limited high sample rate digitised signal, mixes the signal to a lower frequency and reduces the sampling rate while retaining all the information. A DDC will select the frequency band of detection and shift it down in frequency, which allows the data rate required to retain all the information to be much lower, and consequently reduces the complexity of any further processing. A DDC can be split into two main sections, first a digital mixer to frequency shift the spectrum of the signal, and then filters to remove unwanted spectral components and allow reduction, or decimation, of the data rate.

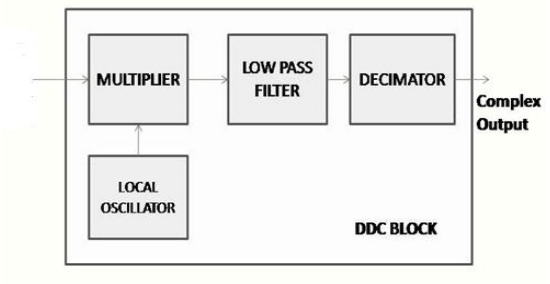


Figure 2: Digital down Converter.

Once each signal has been sampled and converted to a digital data sequence, it is demodulated using a digital detector. Demodulation is performed by multiplying the n^{th} member of the sequence by two coefficients (generated by Oscillator in DDC block), cos ($2\pi f_d n t_s$) and –sin ($2\pi f_d n t_s$) to produce two new sequences which, after low pass filtering, we define as $I_m(nt_s)$ and $Q_m(nt_s)$ respectively. The demodulation frequency, f_d, is the mid frequency of the lowest band (low pass filter as part of DDC block), these I_m and Q_m

are the Inphase and Quadrature components of the received signal respectively. Decimating the sample frequency makes signal processing simpler to implement as the timing constraints can be relaxed. It can also lead to a reduction in the amount of FPGA area required to perform the processing as functions can be performed serially rather than in parallel. The sample rate decimation system shall reduce the sample rate by a factor by 4.

ii. Numerically Controlled Oscillator (NCO)

A Numerically Controlled Oscillator (NCO) can be used to generate the digital mixing signal. The NCO main purpose is to generate the carrier signals (cosine).The main advantage is ROM based techniques will be used for area optimization. The main blocks in NCO are Phase accumulator, Phase Register and Phase to amplitude converter.

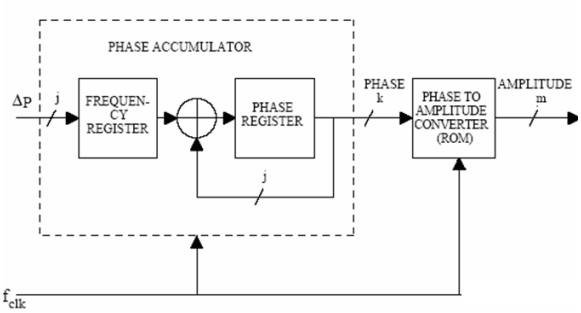


Figure 3: NCO (Oscillator).

iii. Phase Accumulator

The phase accumulator consists of phase increment register, adder and phase register. The phase increment register stores the instantaneous phase increment values resulting from frequency modulation control block. This is fed to an 8 bit adder as one of its input. The other input for adder is phase register output. The phase register holds the instantaneous phase for each clock pulse. The accumulated phase also is represented by 8 bits, which limits the maximum phase by 11111111, and addition by 1 to maximum value causes the phase to become 00000000 this is expected and desired since the Look up Tables are programmed to consider 255 as highest phase value and phase increment by one results next cycle of waveform. Since 8 bits are used to represent the 0^0 to 360^0 the increment in digital phase value by one cause effective increment of 1.40625^0 (results by dividing 360^0 with 256 maximum possible combinations of 8 bits). This also implies that outputs can't have more that 256 samples for one cycle.

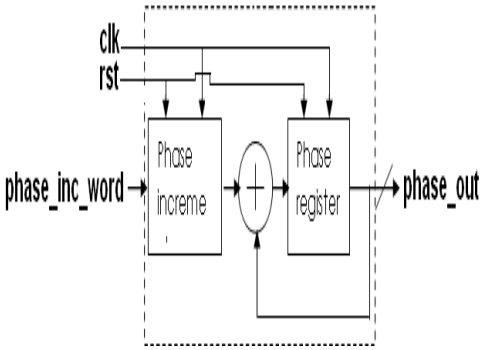


Figure 4: Phase Accumulator.

It can be observed that the resulting phase value after each clock pulse is four added to the previous phase value. The output of phase accumulator is added with multiplier output. That output is given to NCO block. All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency.

IV. SIMULATION RESULTS

The Digital beam forming receiver of phased array radar was simulated using all digital blocks using VHDL coding. In this, we are using the modelsim 6.6b software for simulation results purpose.

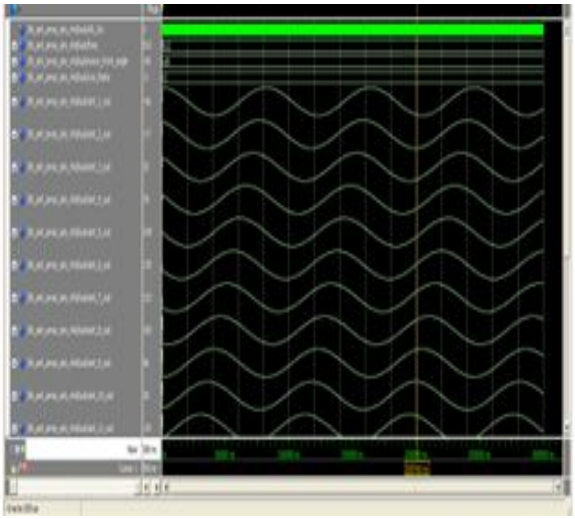


Figure 5: antenna array outputs with phase shifts.

The analog signal is tracked by the Radar antenna as input for processing. Antenna is accept the desired signal and transmits to succeeding block. So the figure 5 shows the continuous wave outputs of the antenna. They are propagated with phase delay. They are given to the RF Translator for translating into inter- mediate frequency. The output of antenna signal is converted to digital form since weighing and summation operations occur at high frequencies in analog beam former where as they are performed at base band frequencies in digital beam former. Figure 6 is similar to the figure 5 but it is digitised one. The thick line shows that the signals are present at high frequencies.

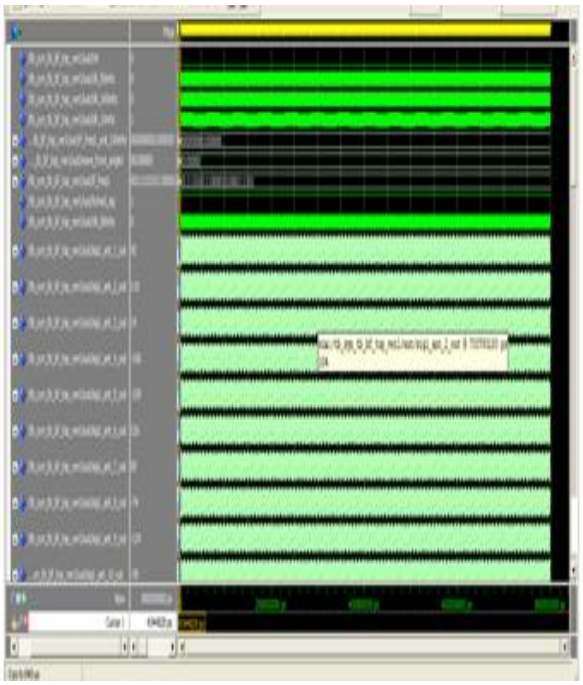


Figure 6: Antenna array outputs in digital form.

High frequency signal is converted to intermediate frequency by Translator. Antenna propagated signal is input for the Translator and low frequency converted signal is the output. The translated signal is shown in figure 7. This is the output of the RF Translator which translates the signal to intermediate frequency of 64MHZ.

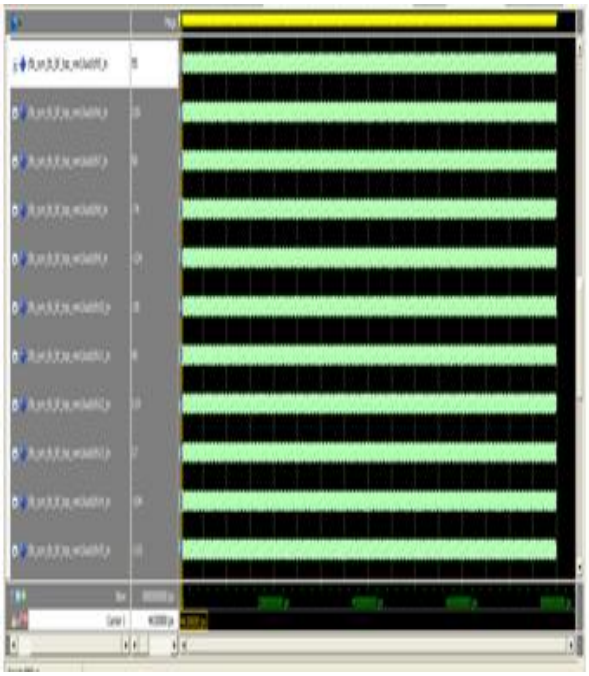


Figure 7: Beam forming inputs.

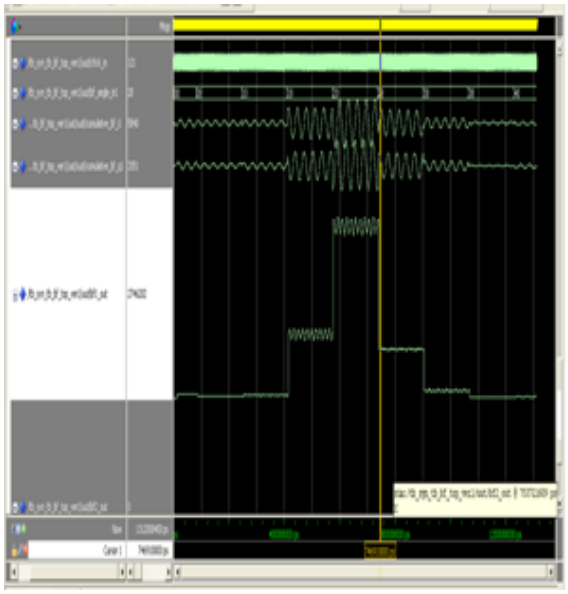


Figure 8: Single Digital Beam output.

Figure 8 is the digital beam formed signal. It is the sum of inphase and quadrature components of the output of the 16 phased array antennas.

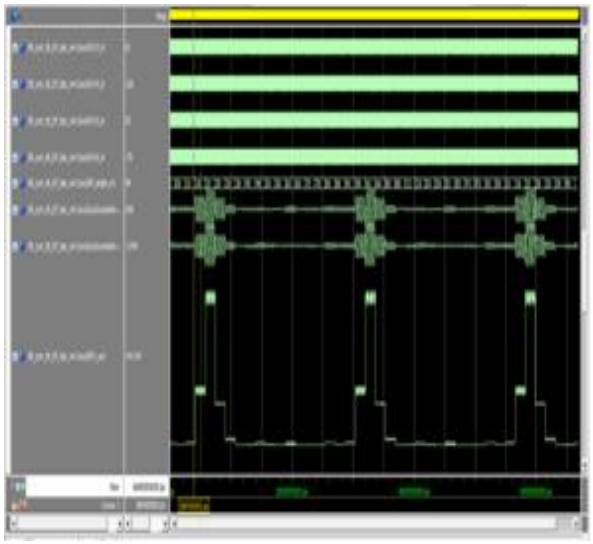


Figure 9: Multiple Digital Beam output.

Figure 9 is the continuous processing of the outputs of 16 phased array antennas. It describes the multiple beam formation by the continuous processing of the 16 antennas.

V.CONCLUSION

The process of beam forming implies weighting these digital signals, thereby adjusting their amplitudes and phases such that when added together they form the desired beam. In this project the design has been explored and implementation of a low-cost digital beam forming platform. The board inputs and FPGA beam forming circuits have been tested to verify system operation. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers and 16 antennas. This technique provides simultaneous beams without any compromise on functionality. The low cost of the system facilitates its easy integration into phased array radar systems.

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