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CMOS BASED CURRENT MODE DEFUZZIFIER CIRCUIT FOR ANALOG FUZZY INFERENCE SYSTEM

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***Abstract*— This paper presents the design of CMOS based defuzzification circuit for Analog Fuzzy Inference system (FIS) application. The defuzzification circuit is implemented using a Multiplier-Divider circuit (MD). The proposed defuzzification scheme is applicable to Takagi-Sugeno systems in which the consequent part of fuzzy rules is singleton values. Center of gravity (COG) is the defuzzification scheme used to convert fuzzy control actions into crisp control signals. The various advantages of the proposed design are - less number of components, high speed operation, wide dynamic range and low power consumption. The performance characteristics and the workability of the proposed circuit are demonstrated using spice simulation.**

***Keywords*— Fuzzy Inference System, Defuzzification circuit, Multiplier-Divider circuit**

I. INTRODUCTION

In the real world there exists much fuzzy knowledge which is vague, imprecise, uncertain, ambiguous, inexact, or probabilistic in nature. A human can process such information because the human thinking and reasoning frequently involve fuzzy information which originates from inherent inexact human concepts and matching of similar rather than identical experiences. The computing systems, based upon classical set theory and two-valued logic, cannot answer to some questions, as human does, because they do not have completely true answers. To overcome this, Fuzzy logic was introduced by L. Zadeh as a means of representing and manipulating data that was not precise, but rather fuzzy [1, 2]. Numerous application of this theory has been implemented in various engineering and non-engineering fields and these successful applications of fuzzy control have sparked a flurry of activities in the analysis and design of fuzzy control systems. Fuzzy control theories have some salient features and distinguishing merits. The different fields in which fuzzy logic has been applied include signal processing, computer vision, automatic control, consumer electronics, house hold appliances, decision making analysis and so on. The number of applications using fuzzy logic techniques to solve control problems has increased considerably. This rapid growth of Fuzzy Logic has motivated the researchers to go for efficient realization of Fuzzy Inference Systems (FIS) [3].

Fuzzy Inference System can be implemented using software or using hardware. Software implementation of FIS is useful when an application can be modelled to simulate and calculate in advance, its multidimensional response characteristic. It provides flexibility as they usually support fuzzy systems with an arbitrary number of rules without any limitation concerning the number, type of membership and range of inference mechanism. On the other hand, it works on a computer or a processor platform and it

has a drawback of being very slow [4, 5]. Hence it is not used for real time application. Therefore hardware realization is preferred for real time applications.

The hardware approach for Fuzzy Inference System can be classified into the following four major categories as reported in the literature – (i) using general-purpose processors, (ii) adapting a general-purpose processor to perform dedicated fuzzy instructions, (iii) using coprocessor or exclusive hardware to perform the fuzzy operations, and (iv) using dedicated fuzzy circuits to implement the entire FIS on a chip. Firstly, the general purpose based FIS design [6] are flexible and involve reduced hardware development time, but at the same time they are not suitable for real time applications and results in a significant amount of overheads. The second method employed for the hardware realization of FIS uses customized classical processors [7] for the execution of some dedicated fuzzy instructions. The approach is a trade-off between speed and generality. The third method used for FIS implementation employs dedicated fuzzy coprocessor [8] to execute specialized fuzzy operations. Here the transfer of control between the main processor and the coprocessor limits the speed of operation. The fourth method uses the design of dedicated circuits for the implementation of Fuzzy Inference Systems. Depending on the design requirements, analog, digital or mixed mode approaches are possible in either voltage or current mode [9]. Each one of them has some advantages and disadvantages that make it suitable for a special purpose. Consideringthe advantages of high accuracy, low power consumption and small chip die size, the analog circuit design is well suited for hardware implementations [10].

The design of dedicated fuzzy controller circuits is however of great interest, because of the increasing number of fuzzy applications requiring highly parallel and high-speed fuzzy processing [11]. Fuzzy controller circuits are designed in a way to optimize fuzzy logic functions as regards to their implementation size and execution speed. Since practical systems often require a great number of rule evaluations per second, a huge amount of real time data processing is necessary and the speed of fuzzy circuits is of prime importance [12]. Depending on the design requirements, analog mode or digital mode approaches are possible. Analog fuzzy system provides high functional density, low power dissipation and high processing speed as compared to digital fuzzy system. It works on continuous time processing so it is compatible with sensors, actuators and other analog signals. Analog implementation has two commonly used process techniques – voltage mode and current mode [13, 14]. Current mode has an advantage over voltage mode as we do not require any adder or differentiator circuits so few number of transistors is used. As compared to voltage mode, current-mode is getting popularity also due to its high speed, low power consumption, large dynamic range, natural form of addition and subtraction and reduced system chip size [15, 16].

The proposed work presents a low power, high speed implementation of a defuzzification circuit which can be used for the CMOS analog design of fuzzy inference system (FIS) to improve the flexibility of analog fuzzy system and make them adaptable to different applications. With the nonlinear characteristics of the active devices in analog circuit, the fuzzy elements can be implemented in very simple structures. This brings a reduction in the circuit complexity which implies better performance and reduced chip area as compared to digital circuitry, even though analog hardware design systems have problem of complexity and modification.

This paper is organized in four sections: Section II describes the proposed architecture of fuzzy inference system. Simulation results are presented in Section III and conclusions are listedin Section IV.

II. THE PROPOSED CIRCUIT

In a fuzzy logic control system there are three main components: (i) Fuzzification (membership function generation), (ii) Fuzzy inference (rule evaluation), and (iii) Defuzzification. This is illustrated in Fig. 1.

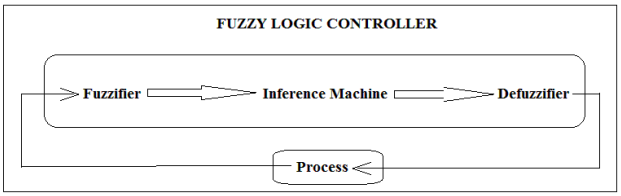

Fig. 1 Fuzzy logic controller block diagram

For the fuzzification process, membership function circuits (MFC) are used to generate Gaussian function, which is one of the most generalized membership functions. The rule evaluation in inference engine is carried out using MIN and MAX circuits.

A. Defuzzification circuit

Defuzzification is an important stage in fuzzy systems, as this block computes crisp output that best represents the fuzzy set obtained as the conclusion. Therefore the entire efficiency of the system is affected by this crisp output. Two of the most common methods are centroid method and maximum area method. Centroid method is the most popular way of defuzzification because it incorporates the contributions of all the rules, analogous with cooperative rule formation strategy.

In this work a new analog CMOS defuzzifier circuit is proposed. The proposed CMOS based defuzzifier is synthesized by multiplier-divider and current replica circuit. Current replica circuit provides many current course scaled value of input current. If input current is I_{in} and output current of i^{th} mirror is I_{oi}. Then,

$$I_{IN} = 0.5K_n'\left(W/L\right)_{IN}(v_{GS} - V_T \qquad (1)$$

$$I_{oi} = 0.5K_n'\left(W/L\right)_i(v_{GS} - V_T \qquad (2)$$

$$I_{oi} = \frac{(W/L)_i}{(W/L)_{IN}} I \qquad (3)$$

$$I_{oi} = \alpha_i I \qquad (4)$$

Where $\alpha_i = \frac{(W/L}{(W/L)}$ and I is transconductance parameter.

B. Multiplier – Divider Circuit

The proposed defuzzification scheme is applicable to Takagi-Sugeno systems in which the consequent part of fuzzy rules is singleton values. The crisp output of defuzzification scheme by center of gravity (COG) is given by

$$y = \frac{\sum_{i=1}^{n} \alpha_i \mu}{\sum_{i=1}^{n} \alpha_i} \qquad (5)$$

Where αi is the weight of the rules, μi is the rule strength, z_i is the singleton values of the consequent part,iis the rule number.

Fig.2 shows the current Multiplier – Divider Circuit. This circuit is based on the translinear principle. Since all of the MOS transistors that comprise the circuit are operated in their sub-threshold region, the dynamic range of the input and output current are limited. The static characteristics of the multiplier – divider is expressed as

$$I_{out} = I_{in}\frac{V_0}{V_0} \qquad (6)$$

V_{OV4} and V_{OV5} are transconductance of amplifier $M_4M_3M_1$ and $M_5M_6M_2$ respectively. In the sub-threshold region override voltage of amplifier is proportional to biasing currents, so we have:

$$I_{out} = I_{in}\frac{I}{I} \qquad (7)$$

Were I_{in} is the input current; I_{B1} and I_{B2} are the biasing currents. By adjusting the bias currents, the proposed circuit works as a multiplier or a divider. If we make I_{B2} as a constant, then the circuit behaves as a multiplier circuit and if we make I_{B1} as a constant, then it behaves as a divider circuit.

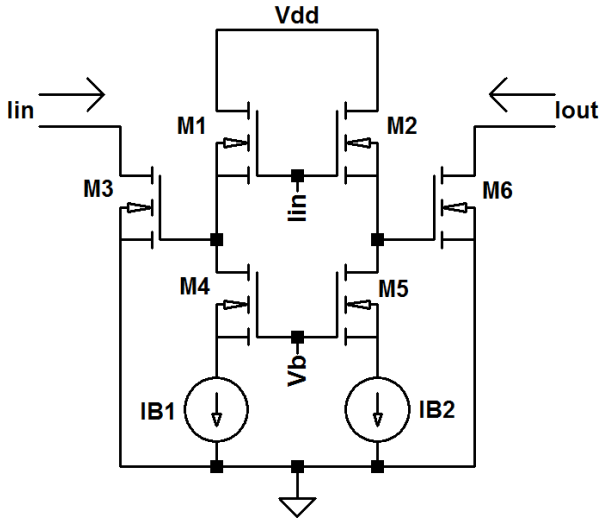

Fig. 2 Current Multiplier – Divider Circuit

C. Defuzzification Scheme

The first stage in the proposed Defuzzifier is current replication circuit which takes the calculated rule strength value as current I_i from inference engine and generates the weighted rule strength current $\alpha_i I_i$. The sum of these weighted rule strength currents produce current $I = \alpha_1 I_1 + \alpha_2 I_2 + \alpha_3 I_3 + \ldots$ The currents $\alpha_i I_i$ and I along with consequent current C_i are fed to the corresponding multiplier – divider circuit. The output of all multiplier – divider are wired to give Defuzzifier output as:

$$I_{out} = \frac{\alpha_1 I_1 C_1}{I} + \frac{\alpha_2 I_2 C_2}{I} + \frac{\alpha_3 I_3 C_3}{I} \qquad (8)$$

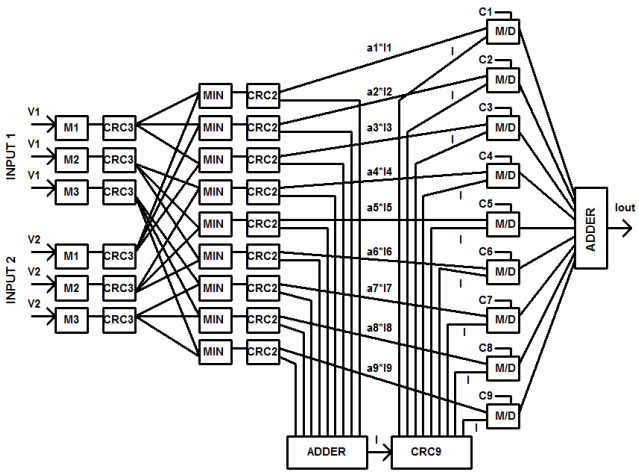

Fig. 3 Block diagram of a 2 – input, 1 – output, 9 – rule Fuzzy Inference System

Figure 3 shows the block diagram of the 2 – input, 1 – output, 9 – rule singleton controller and highlights the three well-known basic fuzzy operations: fuzzification, rule evaluation (inference) and defuzzification. Here M1, M2 and M3 are the membership function circuits, CRC2, CRC3 & CRC9 are the current replication circuits with two, three and nine replications of the input currents respectively, MIN

are minimum circuits to get the minimum of two input currents and M/Ds are the multiplier – divider circuits. All the fuzzy operations mentioned above are performed concurrently.

The choice of zero-order Takagi-Sugeno's architecture is sustained on the good trade-off between simplicity and accuracy that this simple fuzzy algorithm holds. A set of three fuzzy membership functions per input, being shared by several rules, perform the fuzzification operation. At the rule evaluation stage degree of each membership function is replicated through CRC3. After that MIN operation is performed. Since there are three membership functions and two inputs, therefore the number of rules is nine and hence nine MIN circuits are used. At the defuzzifier, each current from inference stage is replicated two times and one of them goes to the input of multiplier-divider circuit and the other to an adder. The adder output is replicated nine times using CRC9 and available as the dividing current in to the multiplier-divider circuit. Also C1, C2, C3,….,C9 consequent currents goes as the multiplying current into the multiplier-divider circuit.

III. SIMULATION RESULTS

The proposed multiplier-divider circuit, shown in Fig. 2, can multiply two currents and divide the same by another current as given by the equation (7). According to the equation, if we make I_{B2} a constant then the circuit behaves as a multiplier, as shown in Fig. 4 & 5 and if we make I_{B1} a constant then the circuit behaves as a divider circuit, as shown in Fig. 6 & 7.

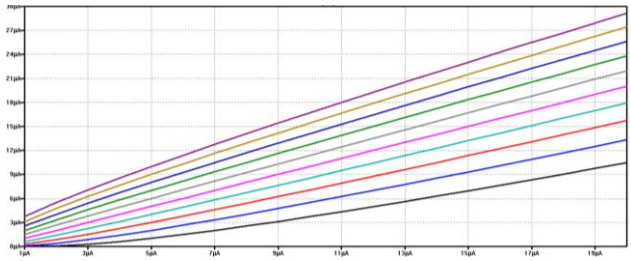

Fig. 4 DC transfer characteristics of Multiplier-Divider circuit where I_{B2} is a constant - a multiplier

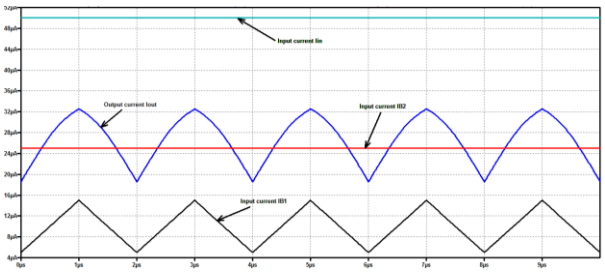

Fig. 5 Transient response of Multiplier-Divider circuit where I_{B2} is a constant - a multiplier

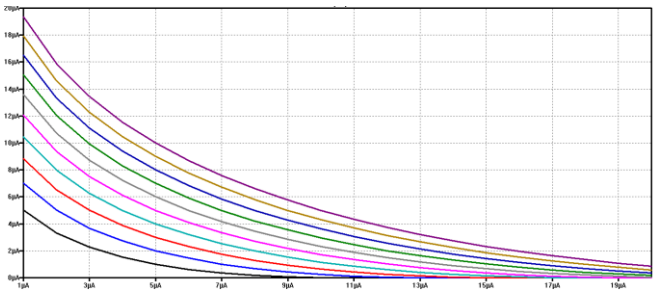

Fig. 6 DC transfer characteristics of Multiplier-Divider circuit where I_{B1} is a constant - a divider

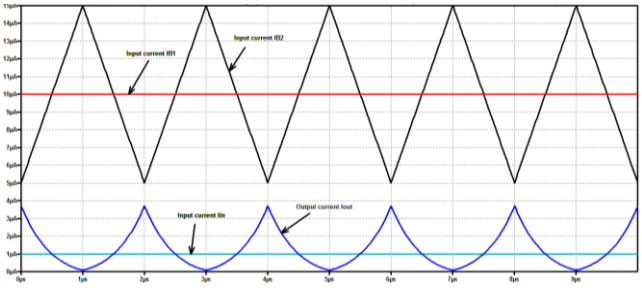

Fig. 7 Transient response of Multiplier-Divider circuit where I_{B1} is a constant - a divider

To verify the function of the Multiplier-Divider circuit, the triangular wave and direct currents were used as its input currents, I_{in}, I_{B1} and I_{B2}. The response shown in Fig. 5 & 7 are obtained by connecting the triangular wave to the input signals I_{B1} (to work as a multiplier) and I_{B2} (to work as a divider) respectively.

Since we consider a zero-order Takagi-Sugeno's controller, the consequents of the rules are singletons. Here an open-loop type of defuzzifier is used since it overcomes the stability problem observed in the closed-loop normalizers due to their inherent feedback. It is thus observed from the multiplier and divider characteristics shown in Fig. 4 to Fig. 7, that the Multiplier-Divider circuit can be used as a means for defuzzification in the proposed Fuzzy Inference System.

IV. Conclusions

In this paper we have presented the design and simulation of the defuzzifier circuit. The circuit have the following characteristics: (i) the programmability in defuzzification stage is obtained by varying the value of αi (weight of the rules) as well as varying the singleton values at consequent part (C_i), (ii) the proposed defuzzifier circuit has simple structure, high processing speed and low power consumption, (iii) this defuzzification circuit is suitable for both analog signal and mixed signal fuzzy inference hardware system, and (iv) since these circuits are implemented using current mode CMOS design it is best suited for IC design technology.

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