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Distribution System Load Forecasting in handling the UI Charges using Neural Network

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Abstract

The BCH (Bose-Chaudhuri-Hocquengem) codes are one of the most powerful algebraic codes, and are extensively used in modern communication system. Many applications of the BCH codes such as long-haul optical communication systems, magnetic recording systems, solid-state storage devices and digital communications require high competing demands, parallel implementation is needed. Since the parallel implementation requires complicated hardware, the design of the area-efficient decoder is very important. The encoding of binary BCH codes consists of the following three steps: i) at first the received polynomial is fed into a syndrome computation block, and generates a syndrome polynomial; ii) then the key equation is solved in the key-equation solver block; iii) eventually, the error are corrected by finding out the roots of error locator polynomials using the Chien search algorithm. The Chien search process is the most complex block in the decoding of BCH codes. Since the BCH codes conduct the bit-by-bit error correction, they often need a parallel implementation for high throughput applications. The parallel implementation obviously needs much increased hardware. In this project, we propose a strength reduced architecture for parallel Chien search process. The proposed method transforms the expensive modulo $F(X)$ multiplications into shift operations, by which not only the hardware for multiplications but also that for additions are much required. The project aims at implementation of an efficient VLSI architectures for Strength Reduce Parallel Chien Search. The main

advantage of implementation using hardware based is its inherent speed over software based methods. The speed is due to flexibility of reconfigurability and reprogram ability of FPGA. This architecture is authored in Verilog; Behavior simulation is done by using the ModelSim 6.0. PAR Simulation can be done by using the synthesis Xilinx ISE 10.1i.

1. Introduction

Digital communication system is used to transport an information bearing signal from the source to a user destination via a communication channel. The information signal is processed in a digital communication system to form discrete messages which makes the information more reliable for transmission. Channel coding is an important signal processing operation for the efficient transmission of digital information over the channel.

It was introduced by Claude E. Shannon in 1948 by using the channel capacity as an important parameter for error – free transmission. In channel coding the number of symbols in the source encoded message is increased in a controlled manner in order to facilitate two basic objectives at the receiver: error detection and error correction.

7. References

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